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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,471	12/04/2001	Dieter E. Staiger	DE919990094US1	7452

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EXAMINER	
NGUYEN, VAN H	
ART UNIT	**PAPER NUMBER**
2126	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/004,471	STAIGER, DIETER E.	
	Examiner	Art Unit	
	VAN H NGUYEN	2126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 are presented for examination.

Specification

2. The disclosure is objected to because of the following informalities:

(i) "Another method used by real-time bus controllers are so called "filter register"" (page 3, line 12) should read "Another method used by real-time bus controllers is so-called "filter register""

(ii) "each bus adapter 214 to 217 possess a connection to a multiplexer 222" (page 8, lines 19-20) should read "each bus adapter 214 to 217 possesses a connection to a multiplexer 222"

(iii) "The intercommunication preprocessor advantageously relieves the load on the master CPU by reducing the workload on the master CPU induced by bridge, router, gateway functions to a minimum" (page 19, lines 23-25) should read "The intercommunication preprocessor advantageously relieves the load on the master CPU by reducing the workload on the master CPU induced by bridge, router, and gateway functions to a minimum"

Applicant is requested to review the entire specification and make appropriate corrections.

Claim Objections

3. Claims 19 and 21 are objected to because of the following informalities:

(i) "whereby said processing is executed sequentially, in parallel both sequentially and in parallel" (claim 19, lines 9-10) should read "whereby said processing is executed sequentially, in parallel, or both sequentially and in parallel"

(ii) "at least on CPU" (claim 21, line 3) should read "at least one CPU"

(ii) "whereby said processing is executed sequentially, in parallel both sequentially and in parallel" (claim 21, lines 10-11) should read "whereby said processing is executed sequentially, in parallel, or both sequentially and in parallel"

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. The following phrases lack antecedent basis:

(i) the device (claim 1, line 2)

(ii) the message processing (claim 1, line 6; claim 19, line 11; and claim 21, line 12)

(ii) the first set of registers (claim 12, lines 1-2)

(ii) said message (claim 12, line 3; claim 19, line 12; claim 21, line 8)

(ii) the intercommunication processing device (claim 15, line 1)

(ii) said switchboard (claims 15-18, line 1)

(ii) the initial step (claim 20, line 1)

B. The following phrases are indefinite:

(iii) a received message (claim 2, lines 2-3; claim 3, line 3; claim 4, line 3; claim 13, line 3; claim 20, line 2) because it is not clear if it is referred to "the received message" claimed in claim 1 (line 4).

(ii) a message (claim 9, line 2; claim 10, line 2; claim 11, line 2; claim 19, line 7) because it is not clear if it is referred to "the received message" claimed in claim 1 (line 4).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by **Kim et al.** (U.S. 4,625,308).

8. As to claim 1, Kim teaches the invention as claimed including a message processing device for communicating with remote units over at least one data network and with at least one dedicated CPU (col.2, line 54-col.3, line 51), the device comprising:

first execution unit for receiving a message to be processed and determining the kind of treatment to be performed with the received message *(e.g., receives messages...examining the message type; col.76, lines 46-61 and col.84, lines 52-67),*

a second execution unit for performing the determined treatment *(e.g., If the message dispatcher task determines that the intended message destination is a lower-level subsystem, the serial subsystem-control subsystem interface task is initiated which decodes the destination field and initiates message transmission to the appropriate serial subsystem. If the task determines that the destination is the control subsystem itself, the message processing task is initiated which evaluates the message data and takes the appropriate action; col.76, lines 46-61/the message processors perform whatever action is required by the message; col.78, lines 8-12)*, and

a third execution unit for presenting the result of the message processing to be forwarded to a destination unit *(e.g., routes required responses to the appropriate destination; col.78, lines 8-12).*

9. As to claim 2, Kim teaches the first execution unit comprises a memory device for storing control information being used to determine the treatment to be performed with a received message (col.33, lines 53-55; col.52, lines 51-56; and col.84, lines 65-66).

10. As to claim 3, Kim teaches the second execution unit comprises a first set of registers for storing message specific information specifying the data contents and the determined treatment of a received message (col.33, lines 31-52; col.34, lines 24-30; and col.83, lines 39-67).

11. As to claim 4, Kim teaches the second execution unit comprises a first set of registers for storing message specific information specifying the data contents and the determined treatment of a received message (col.33, lines 31-52; col.34, lines 24-30; and col.83, lines 39-67).

12. As to claim 5, Kim teaches the second execution unit comprises at least one process execution unit having access to the first set of registers for performing the determined treatment (col.83, lines 39-67).

13. As to claim 6, Kim teaches the second execution unit comprises three or more process execution units having access to the first set of registers for performing the determined treatment (col.83, lines 25-67).

14. As to claim 7, Kim teaches the second execution unit comprises a second set of registers being connected to the at least one process execution unit for storing information needed by the process execution unit (col.33, lines 31-52; col.34, lines 24-30; and col.83, lines 39-67).

15. As to claim 8, Kim teaches the second execution unit comprises a second set of registers being connected to the at least one process execution unit for storing information needed by the process execution unit (col.33, lines 31-52; col.34, lines 24-30; and col.83, lines 39-67).

16. As to claim 9, Kim teaches the second execution unit is configured to monitor the first set of registers in order to start processing a message once a process execution unit is available for processing (col.83, lines 39-67).

17. As to claim 10, Kim teaches the second execution unit is configured to monitor the first

set of registers in order to start processing a message once a process execution unit is available for processing (col.83, lines 39-53).

18. As to claim 11, Kim teaches the second execution unit is configured to monitor the first set of registers in order to start processing a message once a process execution unit is available for processing (col.83, lines 39-53).

19. As to claim 12, Kim teaches the third execution unit is configured to monitor the first set of registers in order to start presenting the result of the message processing once the processing of the message is complete (col.83, lines 54-67).

20. As to claim 13, Kim teaches the first execution unit comprises an interface for configuring the memory device with the control information being used to determine the treatment to be performed with a received message (col.83, lines 39-67 and col.84, lines 52-64).

21. As to claim 14, Kim teaches a switchboard device (col.25, lines 39-56).

22. As to claim 15, Kim teaches a multiplexer connected to the first and third execution unit and for providing connections to several bus adapters and the CPU (col.25, lines 39-48 and col.26, lines 25-36).

23. As to claim 16, Kim teaches an interrupt bus connected to the first execution unit and to several bus adapters and the CPU (col.81, lines 16-25).

23. As to claim 17, Kim teaches a controller for controlling the multiplexer, whereby the controller is configured to be controlled by either the third execution unit or the CPU (col.34, lines 11-14 and col.39, lines 10-13).

25. As to claim 18, Kim teaches a controller for controlling the multiplexer, whereby the controller is configured to be controlled by either the third execution unit or the CPU (col.34,

lines 11-14 and col.39, lines 10-13).

26. As to claim 19, it is directed to a method for presenting the device of claim 1, and is similarly rejected under the same rationale. Additionally, Kim further teaches a first set of registers (col.33, lines 31-52; col.34, lines 24-30; and col.83, lines 39-67) and the processing is executed, among other things, sequentially (col.76, lines 53-col.77, line 2).

27. As to claim 20, Kim teaches storing control information being used to determine the treatment to be performed with a received message (col.84, lines 51-68 and col.100, lines 29-37).

28. As to claim 21, it is directed to a computer program product for implementing the device of claim 1, and is similarly rejected under the same rationale. Additionally, Kim further teaches a first set of registers (col.33, lines 31-52; col.34, lines 24-30; and col.83, lines 39-67) and the processing is executed, among other things, sequentially (col.76, lines 53-col.77, line 2).

Conclusion

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Hitz et al. (U.S. 6065037) teaches "Multiple software-facility component operating system for co-operative processor control within a multiprocessor computer system."

- Saulpaugh et al. (U.S. 5734903) teaches "System and method for object oriented message filtering."

- Ayoub et al. (U.S. 5710924) teaches "Method of routing messages within a multi-processing software system."

- Hillis et al. (U.S. 5590283) teaches "Parallel computer system with physically separate tree networks for data and control messages."

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VAN H. NGUYEN whose telephone number is (703) 306-5971. **After mid-October, 2004, the examiner can be reached at (571) 272-3765.** The examiner can normally be reached on Monday-Thursday from 8:30AM - 6:00PM. The examiner can also be reached on alternative Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (703) 305-9678.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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